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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KHUONG, LEE T	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,683	BENAYOUN ET AL.	
	Examiner	Art Unit	
	Lee Khuong	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☒ Claim(s) *33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6, 8, 11, 14-15, 17-22, 24, 27 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al. (US 6,535,513), hereafter is referred as Kao in view of Riddle (5,166,931).

Regarding claims 1 and 17, Kao teaches a Multimedia and Multi-Rate Switching method and apparatus. Kao teaches a crossbar switch (Fig. 2, 208, ***a cell switching fabric***);

a plurality of LAN adapters coupled for communication therebetween by said crossbar switch (see col. 3, lines 1-11, ***the NMC1 and NMC2, respectively narrowband line cards,***

receive and transmit packets with the cell switching fabric 208), wherein plurality of network adapters includes a serial communication controller (Fig. 2, 212, ***a SCC***) including:

means for converting data frames into serial data (see Fig. 6, 614, ***multi-service engine to convert IP packets/Frames to ATM cells***) before transmitting said serial data to said ATM crossbar switch (see col. 11, lines 54-67, col. 12, lines 1-3, ***packets and frames received from input via attached IP/Frame Relay networks are usually converted to serially concatenated ATM cells prior to being forward to cell switching fabric 208 in Fig. 2***); and

means for converting said serial data (see Fig. 6, 614, ***multi-service engine to convert IP packets/Frames to ATM cells***) received from said crossbar switch into data frames before transmitting said data frame to an attached network (see col. 11, lines 65-67, col. 12, lines 1-3, ***ATM cells received from the cell switching fabric 208,Fig. 2, are converted to packets or frames prior to being transmit to IP/Frame Relay networks***).

Kao does not expressly teach each of plurality of network adapters includes a serial communication controller; means for converting data frames into a bit stream of serial data and means for converting a bit stream of serial data into data frames of parallel bytes.

Riddle teaches a plurality of network adapters (Fig. 1, 110-1 and 110-N, ***LAN Access Modules/LAM***, see col. 2, lines 28-67) includes a serial communication controller, SCC (Fig. 4, 10, ***a serial communication controller***, see col. 7, line 57 – col. 8, line 6); means for converting data frames into a bit stream of serial data (see col. 7, line 57 – col. 8, line 6) and means for converting a bit stream of serial data into data frames of parallel bytes (see col. 7, line 57 – col. 8, line 6).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to employ the LAN Access Module as taught by Riddle into Kao to arrive the claimed invention as specified in claims 1 and 17.

The suggestion/motivation for doing so would have been to provide a seamless communication between different transport format packets/frames between internetwork communications (see col. 1, lines 16-18).

Regarding claims 2 and 18, Kao and Riddle teach all limitations set forth in the rejections of claims 1 and 17. Riddle further teaches each of said plurality of network adapters includes: a control logic (Fig. 4, 20, ***a processor***) for generating a request signal (REQ) to said crossbar switch when said adapter requests transfer of data frames to another network adapter (see col. 8, lines 7-34 and col. 2, lines 28-67, col. 15, lines 55-63).

Regarding claims 3 and 19, Kao and Riddle teach all limitations set forth in the rejections of claims 2 and 18. Riddle further teaches each of said plurality of network adapters capable of including: a clock multiplier (Fig. 4, 30, ***a clock timer***) for multiplying a data clock and for providing said control logic (Fig. 4, 20, ***the processor***) with timing pulses utilized to transmit said request signal (REQ) (see col. 7, lines 34-45 and col. 8, lines 54-59).

Regarding claims 4 and 20, Kao and Riddle teach all limitations set forth in the rejections of claims 2 and 18. It is inherently that a request signal (REQ) includes first data bytes defining a destination address of data to be transmitted in its network layer. Riddle also teaches

second data bytes representing a connection time (***a connection interval***) defined by a number of slots of said crossbar switch in which the data are to be transmitted (see col. 7, lines 34-45).

Regarding claims 5 and 21, Kao and Riddle teach all limitations set forth in the rejections of claims 4 and 20. Riddle further teaches said first data bytes designate a broadcast connection (see col. 8, lines 46-53, ***broadcast***).

Regarding claims 6 and 22, Kao and Riddle teach all limitations set forth in the rejections of claims 1 and 17. Kao further teaches said means for converting data frames into a bit stream of serial data comprises: means for generating serial data in a high-level data link control (HDLC) format, before transmitting said serial to said crossbar switch (see col. 11, lines 54-67, col. 12, lines 1-9).

Regarding claims 8 and 24, Kao and Riddle teach all limitations set forth in the rejections of claims 6 and 22. Kao further teaches said means for converting a bit stream of serial data received from said crossbar switch into data frames comprises: means for converting serial data received from the crossbar switch in a high-level data link control (HDLC) format into LAN data frames (see col. 11, lines 54-67, col. 12, lines 1-9).

Regarding claims 11 and 27, Kao and Riddle teaches all limitations set forth in the rejections of claims 1 and 17. Riddle teaches each of said plurality of network adapters (Fig. 2, 110-1, 110-N) further includes:

an internal parallel bus (Fig. 4, 15, ***a parallel bus***) coupled to the serial communication controller (Fig. 4, 10, ***the SCC***); and

a network controller (Fig. 4, 20, ***a processor***), coupled to the internal parallel bus, for converting received in serial format from an attached network into parallel data bytes and fro transmitting the parallel data bytes to the serial communication controller via the internal parallel bus (see col. 7 line 46 – col. 8, line 59).

Regarding claims 14 and 30, Kao and Riddle teach all limitations set forth in the rejections of claims 11 and 27. Kao further teaches an arbiter (Fig. 8, 814, ***an arbitrating host port interface***) for taking care of the contention between requests to send from said LAN controller and requests to send from said serial communication controller (see col. 15, lines 32-37).

Regarding claims 15 and 31, Kao and Riddle teach a data transmission system set forth in the rejections of claims 1 and 17. Kao further teaches a scheduler for scheduling data transmission between attached networks based upon requests to transmit received from said plurality of adapters (see Fig. 5, 514, col. 9, lines 1-14, ***a controller to decide whether or not to schedule a transfer of the next data***).

4. Claims 7, 9-10, 12-13, 23, 25-26 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Riddle and further in view of Wallace (US 6,252,887 B1).

Regarding claims 7 and 23, Kao and Riddle teach all limitations set forth in the rejections of claims 6 and 22. Riddle further teaches means for generating a first flag to start a data frame (see col. 7, lines 65-68); means for serializing a plurality of incoming parallel data bytes (see col. 7, line 57 – col. 8, line 6); means for cyclic redundancy error checking scheme (see col. 7, lines 63-66) and means for generating a second flag to end the data frame (see col. 7, lines 65-68).

Kao and Riddle do not expressly teach means for computing a frame check sequence (FCS) after said plurality of incoming parallel data bytes.

Wallace teaches means for computing a frame check sequence (FCS) after said plurality of incoming parallel data bytes (see col. 3, lines 48-65, ***a frame relay includes a FCS field***).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the delimiter start and end flags of a frame and the FCS field of Wallace within the ATM switch of Kao and the SCC adapter of Riddle for ensuring the transmission of a frame between frame relay and ATM networks and thus guarantee high-speed, low-error rate data communications.

The suggestion/motivation for doing so would have been to provide transparent communication between a frame relay and an ATM network (see col. 2, lines 4-6).

Regarding claims 9 and 25, Kao and Riddle teach all limitations set forth in the rejections of claims 8 and 24. Kao and Riddle do not expressly teach means for checking the data integrity of said HDLC frame by computing a frame check sequence (FCS) (see col. 3, lines 48-65)

Wallace further teaches means for checking the data integrity of said HDLC frame by computing a frame check sequence (FCS) (see col. 3, lines 48-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the delimiter start and end flags of a frame and the FCS field of Wallace within the ATM switch of Kao and the SCC adapter of Riddle for ensuring the transmission of a frame between frame relay and ATM networks and thus guarantee high-speed, low-error rate data communications.

The suggestion/motivation for doing so would have been to provide transparent communication between a frame relay and an ATM network (see col. 2, lines 4-6).

Regarding claims 10 and 26, Kao, Riddle and Wallace teach all limitations set forth in the rejections of claims 9 and 25. Riddle further teaches a memory including network-to-switch area organized in a first plurality of buffers for storing data to be transmitted via said crossbar switch, (Fig. 4, 30, ***a first RAM to store input data 111-1. The first RAM 30 of Fig. 4 is inherently comprises multiple buffers which stores received data from 111-1 to be transmitted to the virtual circuit switch 140 and to another LAM or TAM***, see col. 2, lines 28-68, col. 3, lines 6-7, col. 5, lines 22-42, 53-65 and col. 8, lines 7-30), and a switch-to-network area organized in a second plurality of buffers for storing data received from said crossbar switch (Fig. 4, 30, ***a second RAM to store output data of 111-N or 210-1. The second RAM 30 of Fig. 4 is inherently comprises multiple buffers which stores data to be transmitted from the virtual circuit switch 140 to another attached network 300-5***, see col. 2, lines 28-68, col. 3, lines 6-7, col. 5, lines 22-42, 53-65 and col. 8, lines 7-30).

Regarding claims 12 and 28, Kao and Riddle teach all limitations set forth in the rejections of claims 11 and 27. Riddle further teaches wherein said network controller further includes: a clock circuit (Fig. 4, 30, ***a timer clock to synchronize operation of data conversion***); means for synchronizing said clock circuit during a set of preamble bytes when receiving an incoming data frame from an attached network (see col. 7, lines 57-68 and col. 8, lines 54-59); and means for deserializing a set of remaining incoming bits of said LAN data frames to provide a set of parallel data bytes (see Fig. 4, 10, **the *SCC***, col. 7, line 57 – col. 8, line 6, ***a mean for converting parallel data to serial data and serial data to parallel data***).

Kao teaches means for removing a set of protocol information of said LAN data frame (see Fig. 6, 610, ***a SAR engine***, col. 11, lines 35-37, ***a SAR engine to performs segmentation and reassembly frames and cell forwarding; adding/removing headers and trailers of ATM protocol***).

Kao and Riddle do not expressly teach means for detecting the incoming data frame through a delimiter byte; and means for checking data integrity of said LAN data frame by computing a set of frame check sequence (FCS) bytes.

Wallace teaches means for detecting the incoming data frame through a delimiter byte (see col. 5, lines 14-22, ***means for detecting starting of an HDLC frame***); means for checking data integrity of said LAN data frame by computing a set of frame check sequence (FCS) bytes (see Fig. 4, col. 3, lines 48-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the delimiter start and end flags of a frame and the FCS field of Wallace within the ATM switch of Kao and the SCC adapter of Riddle for ensuring the transmission of a frame between frame relay and ATM networks and thus guarantee high-speed, low-error rate data communications.

The suggestion/motivation for doing so would have been to provide transparent communication between a frame relay and an ATM network (see col. 2, lines 4-6).

Regarding claims 13 and 29, Kao and Riddle teach all limitations set forth in the rejections of claims 11 and 27. Kao teaches means for generating the protocol information bytes to be included in said an outgoing data frame (see Fig. 6, 614, ***the multi-service engine converts ATM cells back to packets to be forwarded to its attached IP/Frame Relay networks by the packet controller 618***).

Riddle teaches means for serializing a set of incoming data bytes received from said serial communication controller (see Fig. 4, 10, ***the SCC***, col. 8, lines 3-6, ***a mean for converting parallel data to serial data and serial data to parallel data***).

Kao and Riddle do not expressly teach means for computing a frame check sequence (FCS) of said outgoing data frame before transmitting said outgoing data frame on an attached network.

Wallace teaches means for computing a frame check sequence (FCS) of said outgoing data frame before transmitting said outgoing data frame on an attached network (see Fig. 4, col. 3, lines 48-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the delimiter start and end flags of a frame and the FCS field of Wallace within the ATM switch of Kao and the SCC adapter of Riddle for ensuring the transmission of a frame between frame relay and ATM networks and thus guarantee high-speed, low-error rate data communications.

The suggestion/motivation for doing so would have been to provide transparent communication between a frame relay and an ATM network (see col. 2, lines 4-6).

5. Claim 16 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Riddle and further in view of Hughes et al. (US 6,747,971 B1), hereafter is referred as Hughes.

Regarding claims 16 and 32, Kao and Riddle teach all limitations set forth in the rejection of claims 15 and 31. Kao and Riddle do not expressly teach said scheduler further includes: an algorithm unit for determining the best data connection to establish based upon selection of a request amongst all requests concurrently received from said plurality of adapters which meets a predetermined criterion.

Hughes teaches wherein said scheduler further includes: an algorithm unit (Fig. 3, 314, ***the request controller***) for determining the best data connection to establish at each time based

upon the selection of the request amongst all requests received from the LAN adapters which meets predetermined criteria (see col. 10, lines 32-50, ***the request controller will identify the cells with head-of-line priority and a generates primary service request***).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the scheduler of Hughes within the ATM switch of Kao and Riddle for controlling input/output traffic within an ATM switch to avoid network congestion.

The suggestion/motivation for doing so would have been to provide a reliable communication between a frame relay and an ATM network (see col. 2, lines 4-5).

Allowable Subject Matter

6. Claims 33 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1 and 17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Witsaman et al. (US 5,369,682); Huscroft et al. (US 6,188,692); Thurston (US 6,738,392); are cited to show The System for Transmitting Local Area Network (LAN) Data Frames Through an Asynchronous Transfer Mode (ATM) Crossbar Switch, which is considered pertinent to the claimed invention.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lee Khuong whose telephone number is 571-272-3157. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lee T. Khuong
Examiner
Art Unit 2665

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